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High Power CW and QCW Diode Monolithic Stack Technology Overview

Mark Mondry

Outline

- **Bar Technology**
  - 808 nm AAA™ "Extended Power" Bars
  - 9xx nm High Efficiency Bars
- **Stack Technology**
  - Conductively Cooled "G-stack" – Gen 4
  - Silicon Monolithic Microchannels (SiMMs)
- **On The Horizon**

Bar Technology

808 nm AAA™ "Extended Power" Bars

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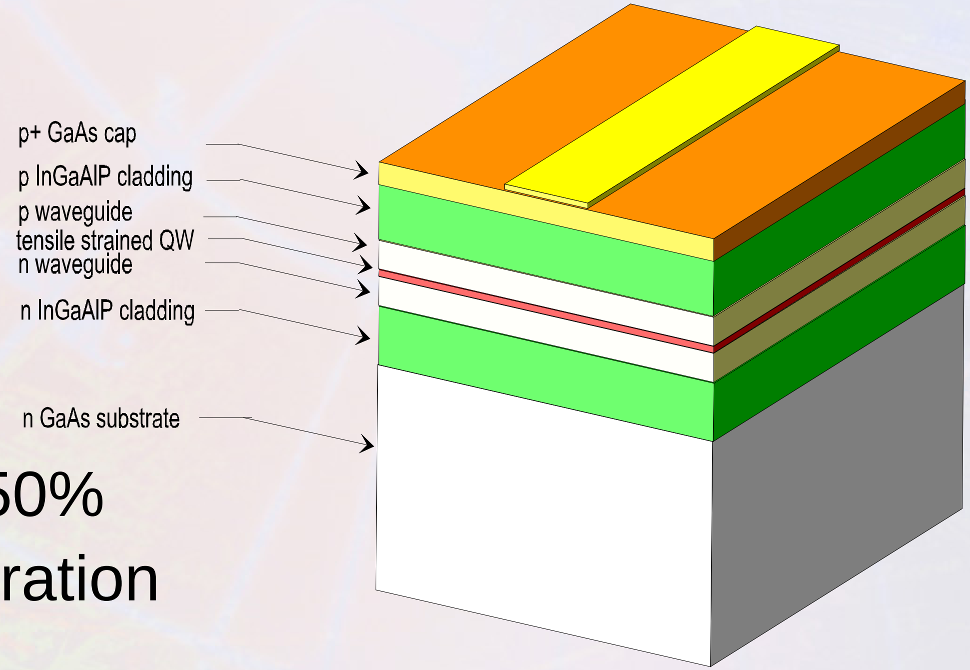
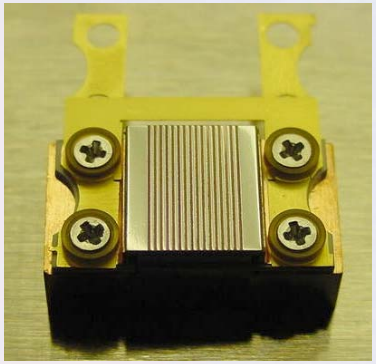
Aluminum-free Active Area – The AAA™ Advantage



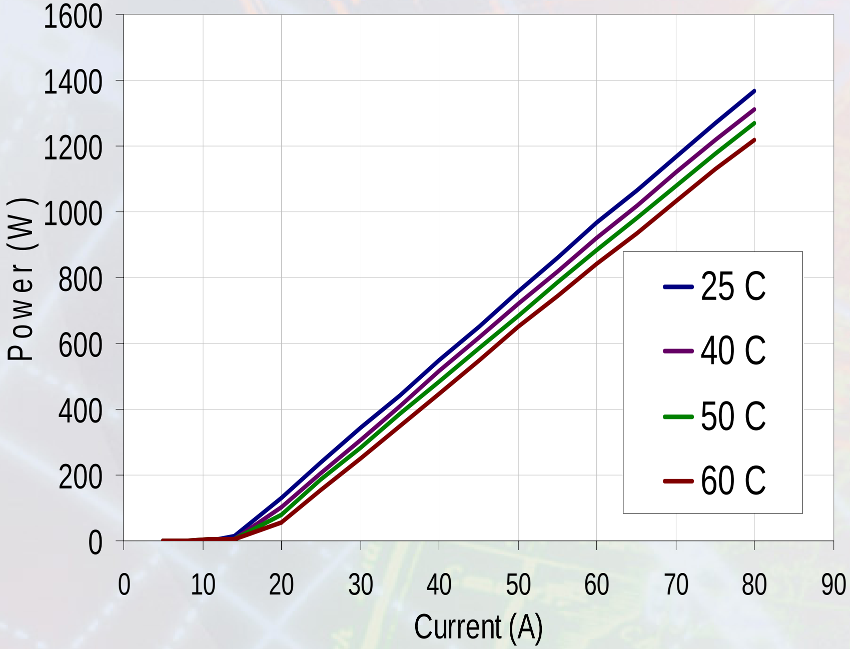
- **High Performance**
  - Conversion efficiencies >50%
  - Elevated temperature operation
- **MBE Grown**
  - High degree of uniformity and reproducibility
- **Intrinsic Long Lifetime**
  - Aluminum-free region eliminates failure mechanisms associated with AlGaAs lasers.

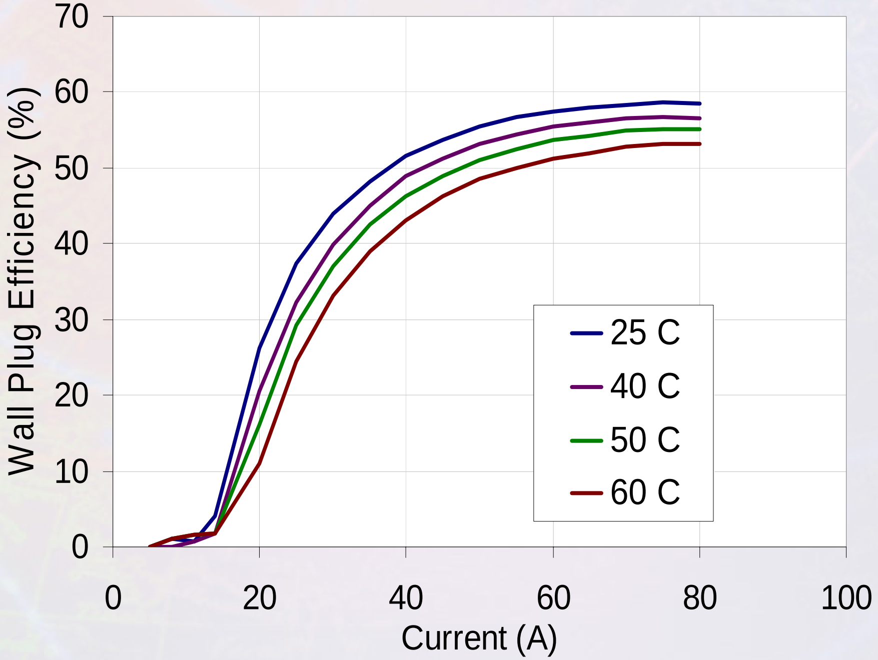
High Temperature Performance



Conductive-cooled 16 bar "G-stacks"

250 μsec pulses @ 0.5% duty cycle

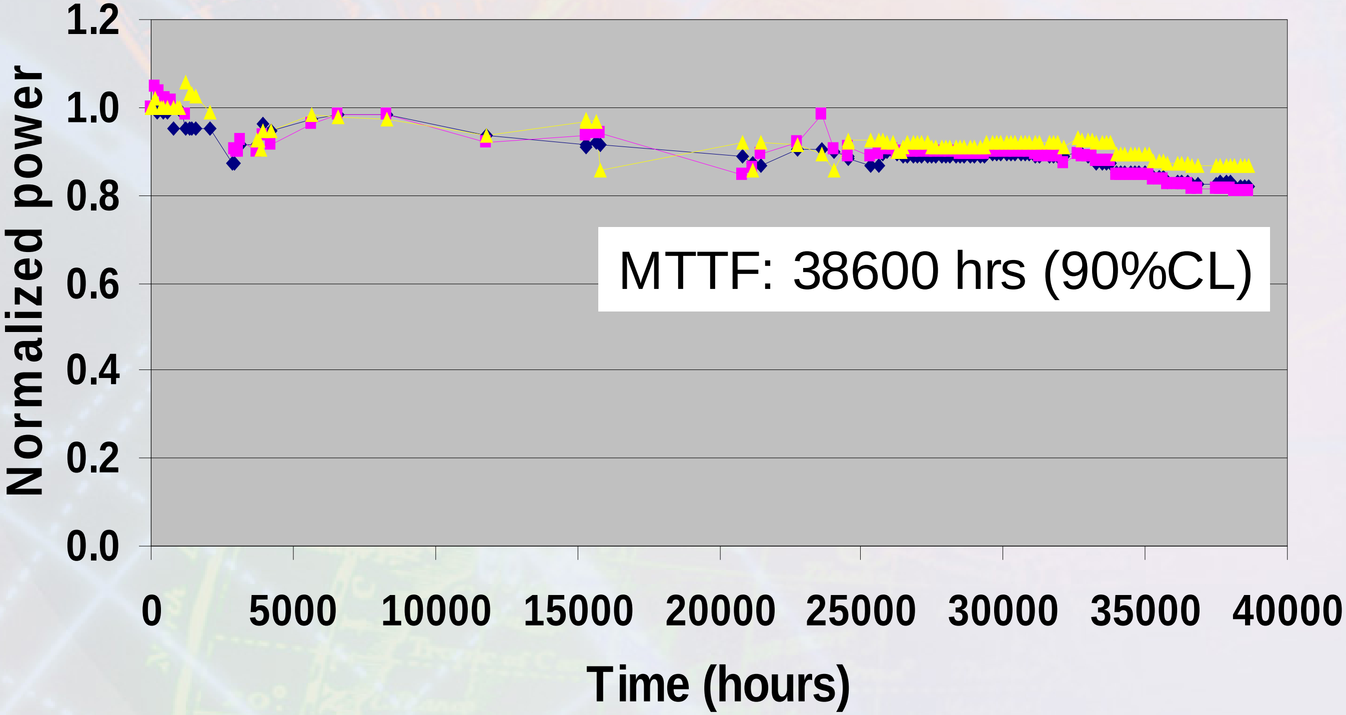




Wall Plug Efficiency @ 808 nm >50% @ 60° C

Aluminum-free Active Area (AAA™) Reliability

90% FF 0.6 mm cavity on conductively-cooled package
80 Amps Constant Current (80 W) at 25° C
200 μsec pulses @ 25% duty cycle



Limitations of Traditional Epi Design

- **Define device operating power in terms of linear power density:**

$$\mathrm{LPD} = \frac{P_{op}}{\text{width of active region}}$$

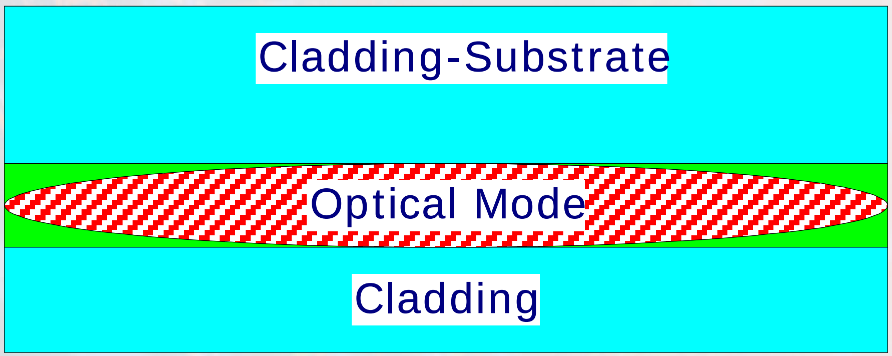
- **We observe limited reliability for LPD ≈ 20 mW/μm for our traditional design**

- **Challenge:**

How to increase the reliable operating power density while maintaining the high confidence of product consistency?

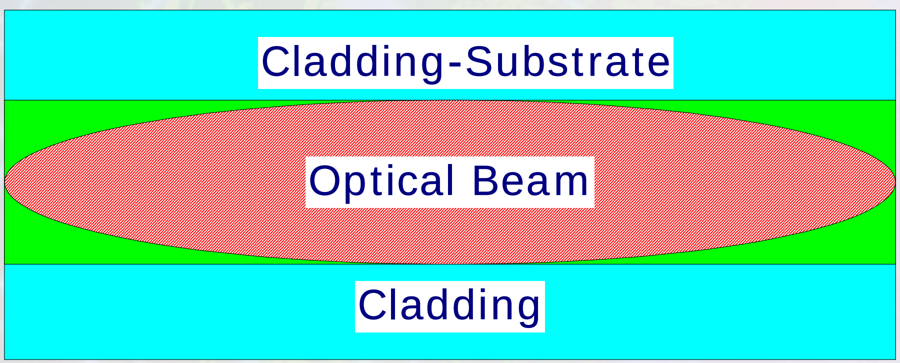
Answer: A vertical scaling of the epitaxial structure

Traditional Design



Traditional waveguide designed to support single transverse mode

"Extended Power" Design

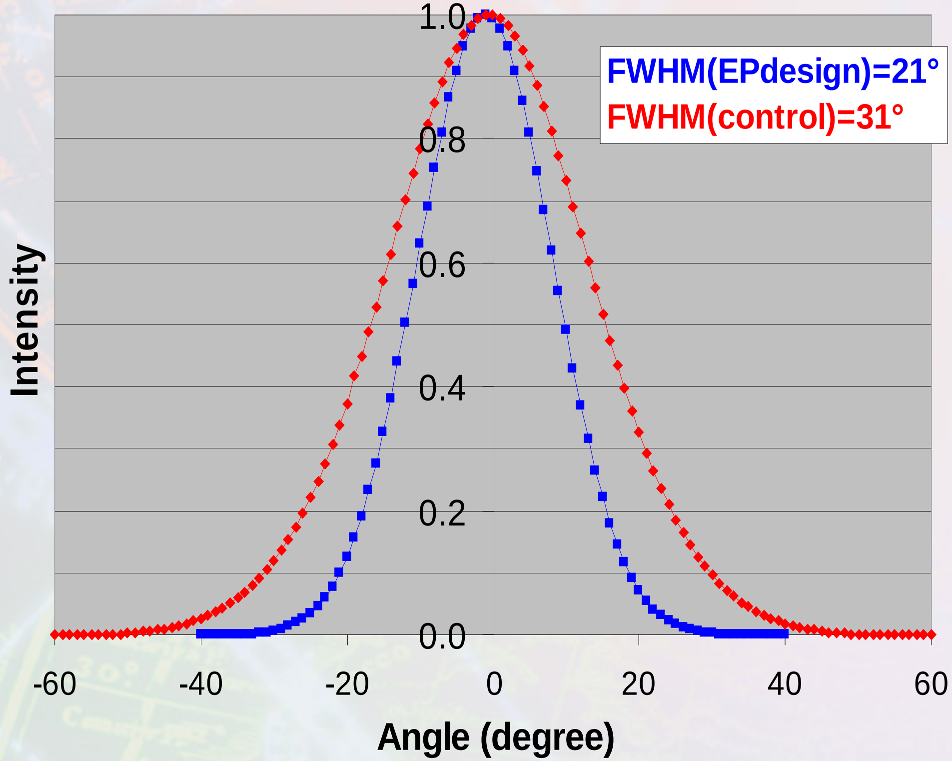


EP design increases the waveguide thickness and expands the optical mode

Benefits of “Extended Power” Epi Design

- No new processing – minimizes fabrication complexity and new failure mechanisms
- Increases Castrophic Optical Damage (COD) Limit
- Lower Cavity Photon Density
- Extends the Reliable Operating Power Limit of our AAA™ technology
- Improved Output Beam Characteristic (fast axis)

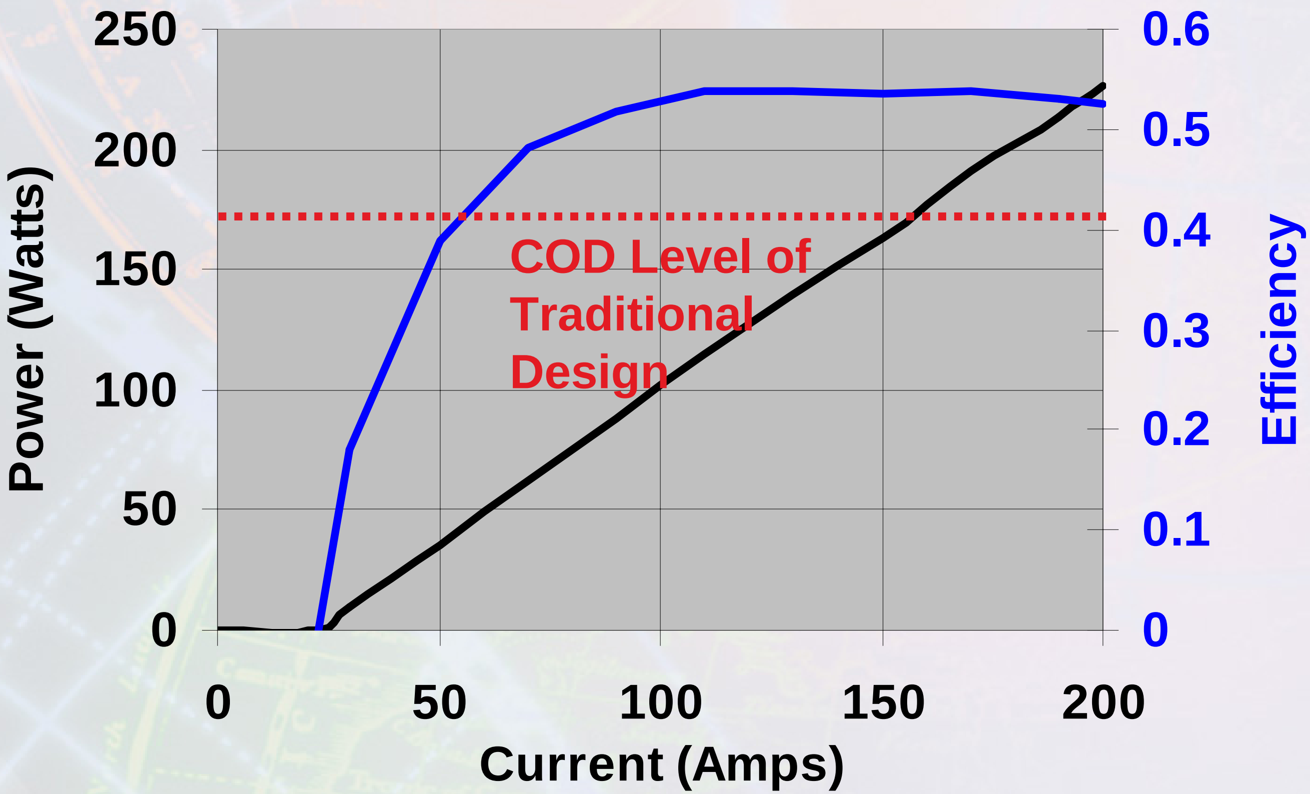
Reduced Fast Axis Divergence – EP Design



- ➢Reduced divergence enables lower cost lensing and potentially improves power coupling

QCW Device Performance

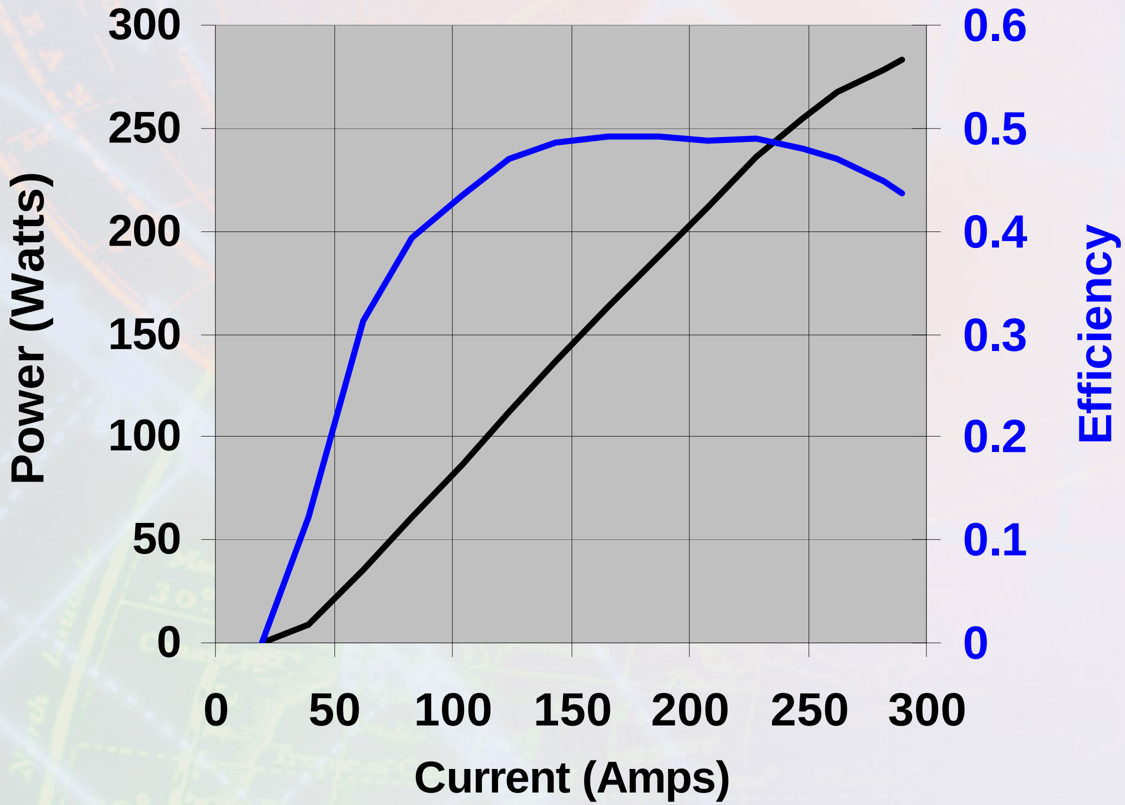
90% FF 1.0 mm cavity length tested on conductively cooled package with 200us pulse @ 100Hz at 20° C



➢**WPE is 53% @ P_{op}=200 Watt**

QCW Device Performance

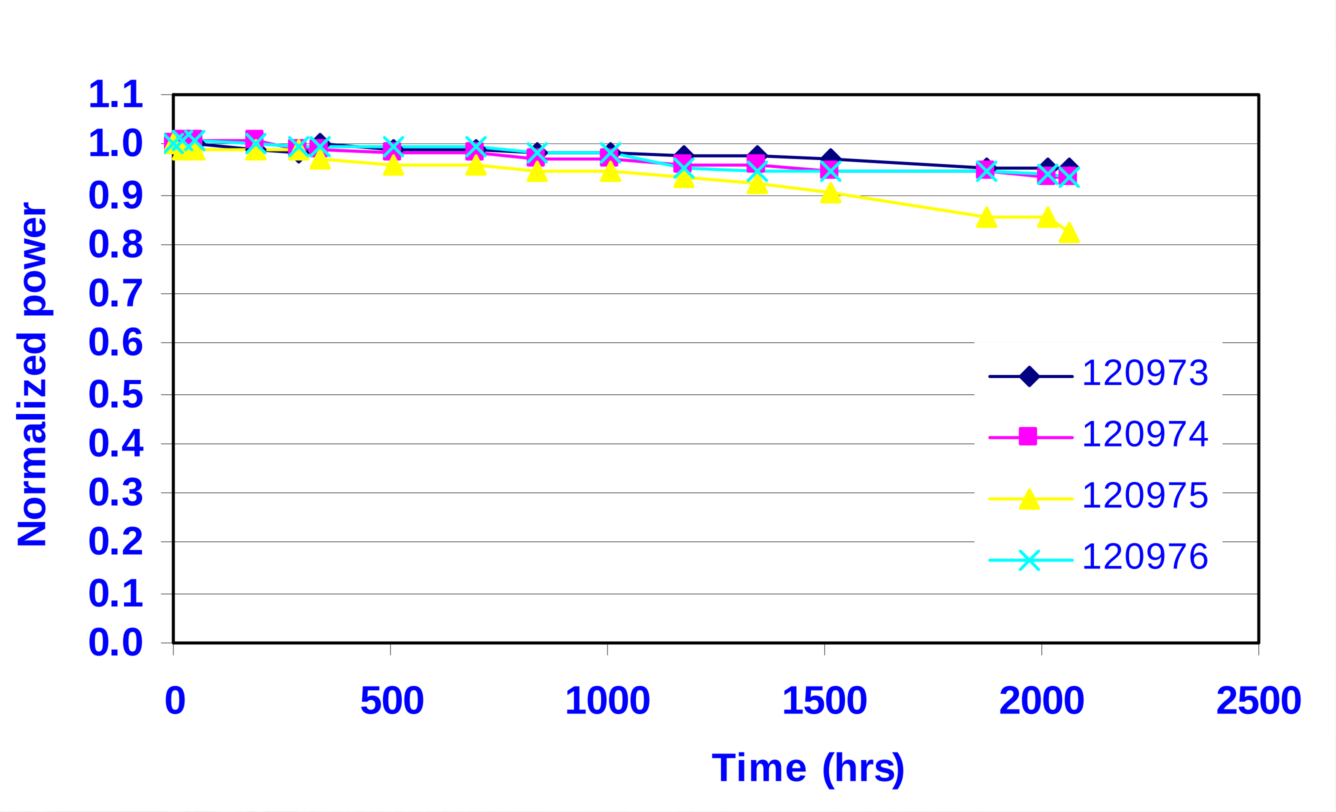
90% FF 1.5 mm cavity length tested on conductively cooled package with 500us pulse @ 50Hz at 25 ° C



- **270 watts with an efficiency of 45%**

QCW Device Reliability

“Half bar” 90% FF 1.5 mm cavity length devices tested at 150 A on conductively cooled package with 500us pulse @ 200Hz at 25° C



➢**At 270 W/cm, MTTF:4271hrs or 3.2e9 shots (90%CL)**

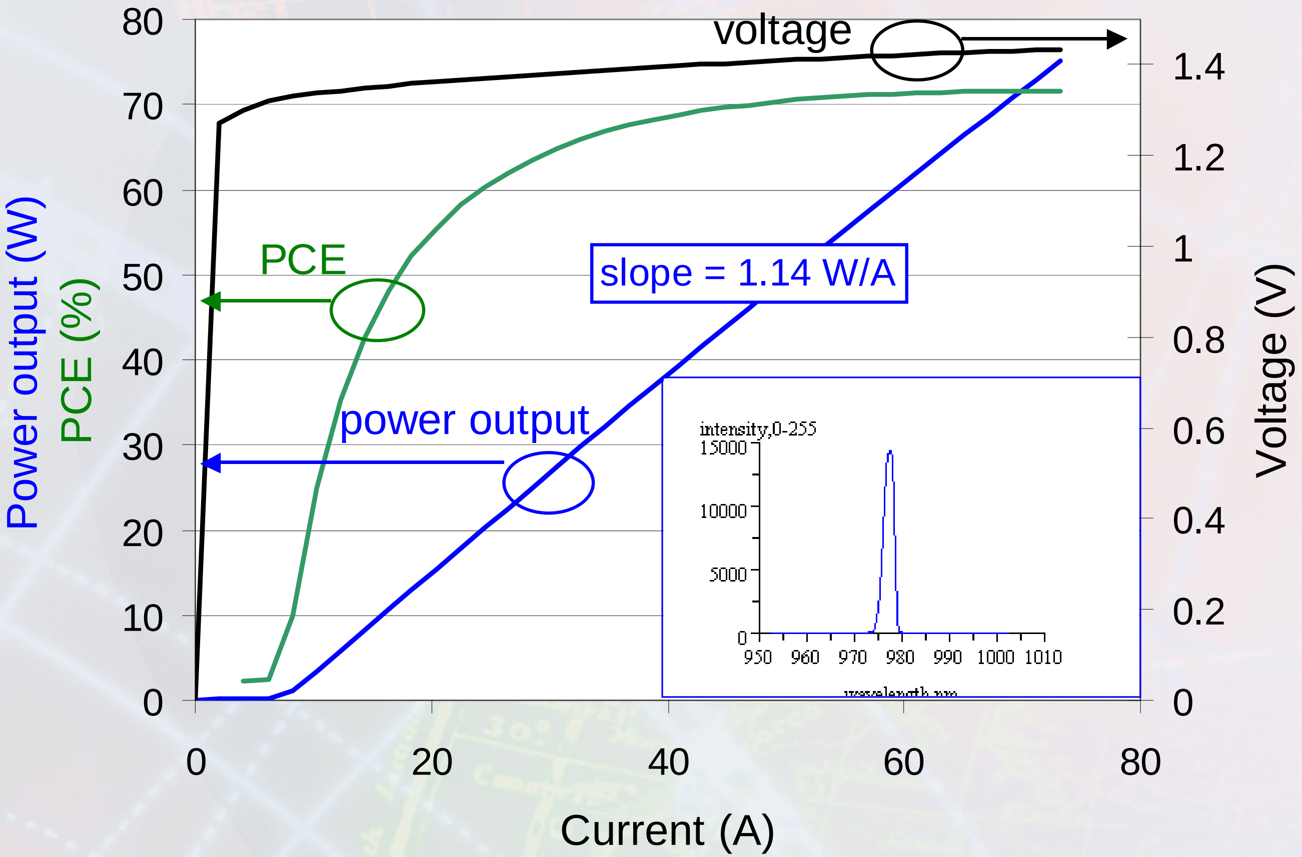
Bar Technology

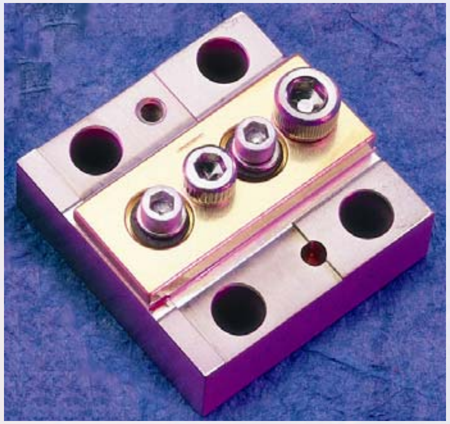
9xx nm High Efficiency Bars

Coherent 9xx nm Bar Technology

- **New semiconductor material system for Coherent**
  - more optimized for 9xx nm than our AAA™ material
- **Development started in early 2004**
  - First report of >60% wall plug
- **Emphasis has been on manufacturability rather than “hero” results**

Efficiency of our 9xx nm conductively-cooled bars

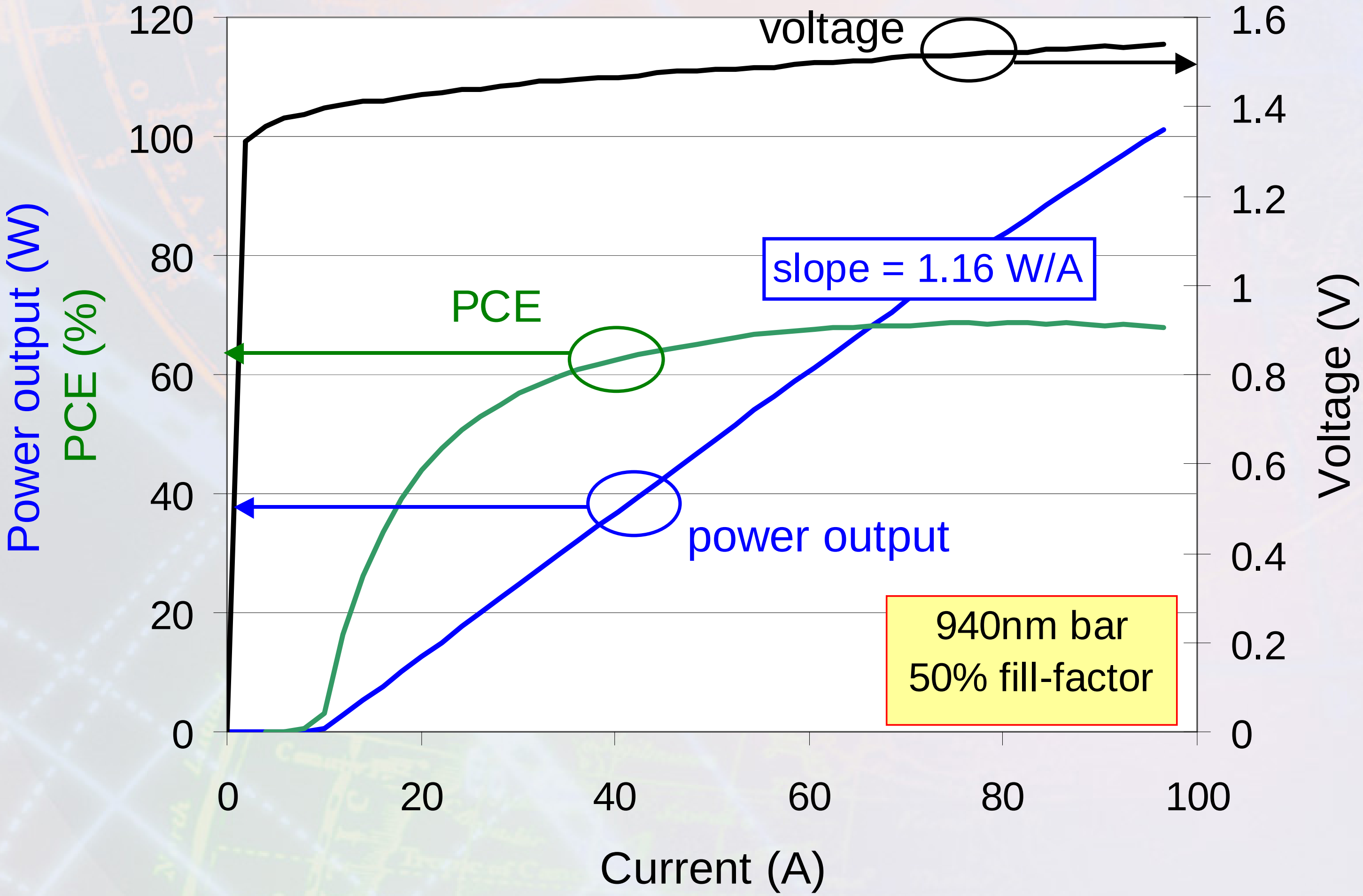




71.5% power-conversion-efficiency at 70 watts CW

for 30% FF 1.5 mm cavity length bar

Efficiency of our 9xx nm conductively-cooled bars



50% 940 nm bars exhibit 68.2% efficiency at 100 W CW

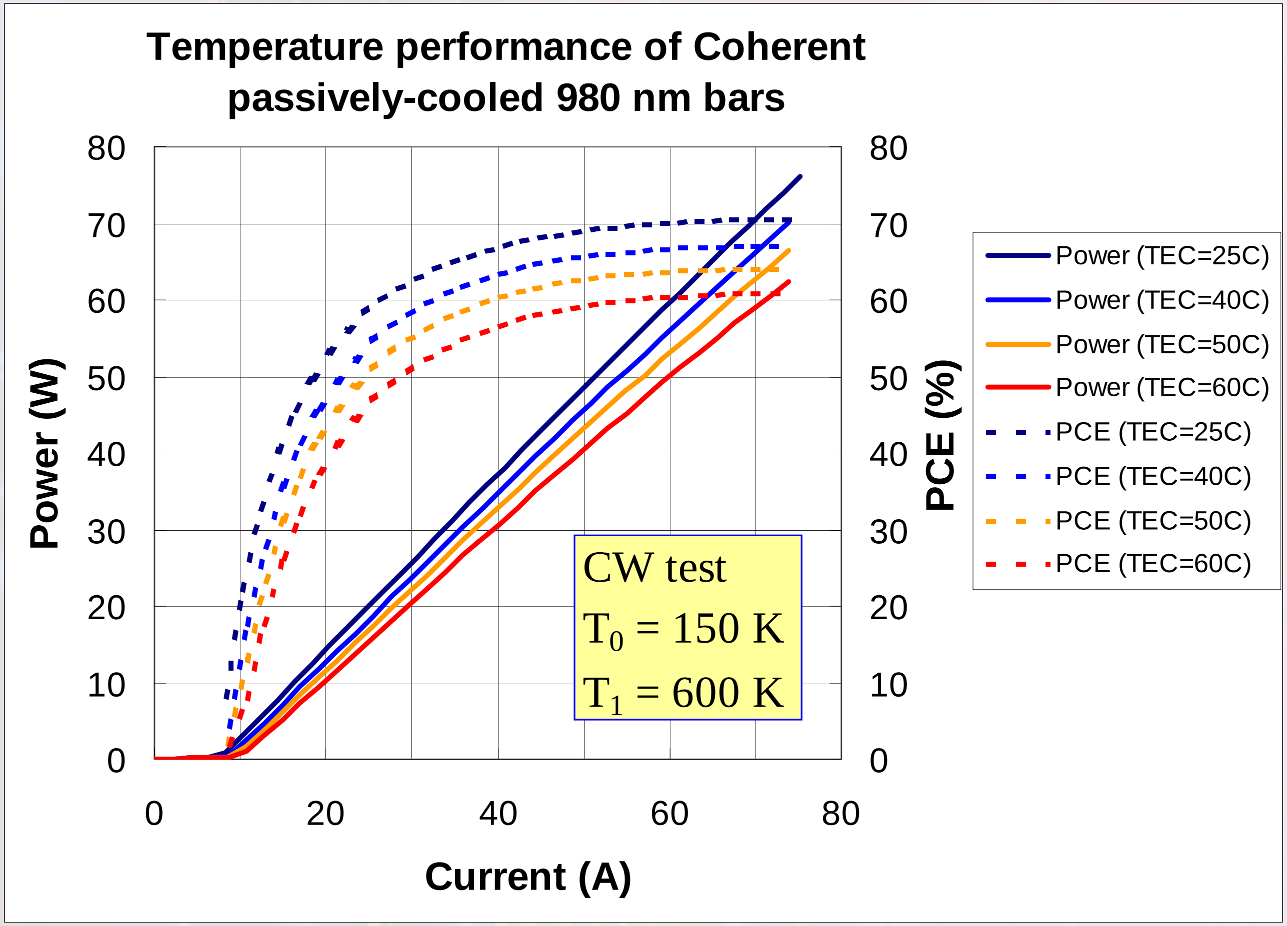
Performance Comparison of Coherent bars versus SHEDS program

Attribute	JDSU	nLight Photonics	Alphalight	Coherent
Bar Power Output	87.9 W	89.6 W	81.4W	75 W with 30% FF bars; 100 W with 50% FF bars
Cool Type	Active water cooling	Active water cooling	Active water cooling	Passive conduction cooling
Bar Power Conversion Efficiency	65.3%	64.1%	64.7%	71.5% at 75W; 68.2% at 100W
Reliability at this power & geometry	unknown	unknown	unknown	MTTF > 20,000 hours for 75W bars. Reliabilty test in progress for 100W bars
Junction Temperature	50.7°C	49.5°C	51.1°C	40°C at 75 W; 50.5°C at 100 W
Spectral Width	3.8 nm	0.8 nm	3.5 nm	3.5 nm

"Real World" Efficiencies of 9xx nm CCP products in manufacturing

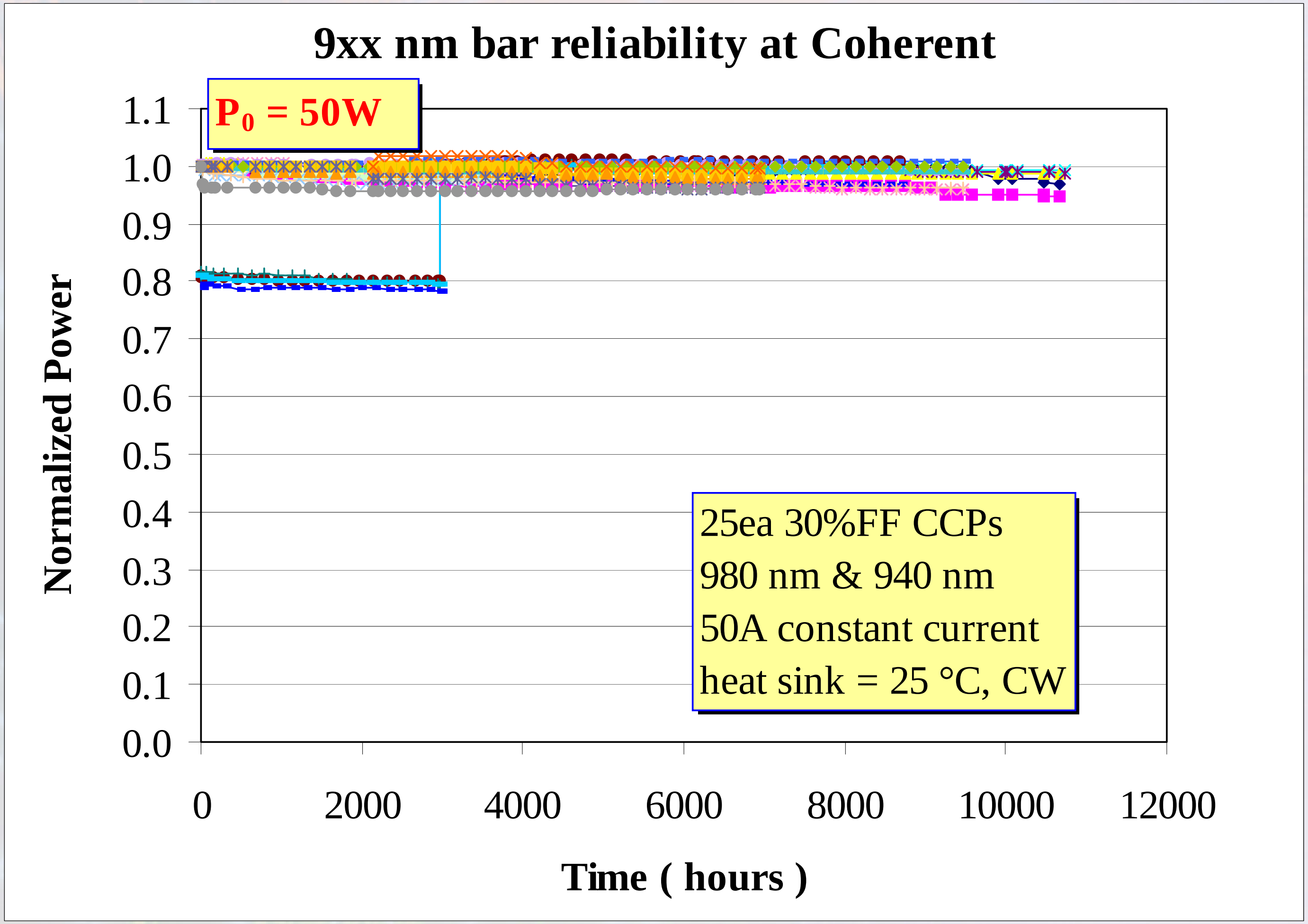
Test Condition: (CW @ TEC = 25 ºC, passively cooled)	Highest CCP PCE	Typical CCP PCE tested in factory
980 nm	71.5%	66%
940 nm	69.5%	65%
915 nm	67.0%	64%

Efficiency of our 9xx nm bars at elevated temperatures

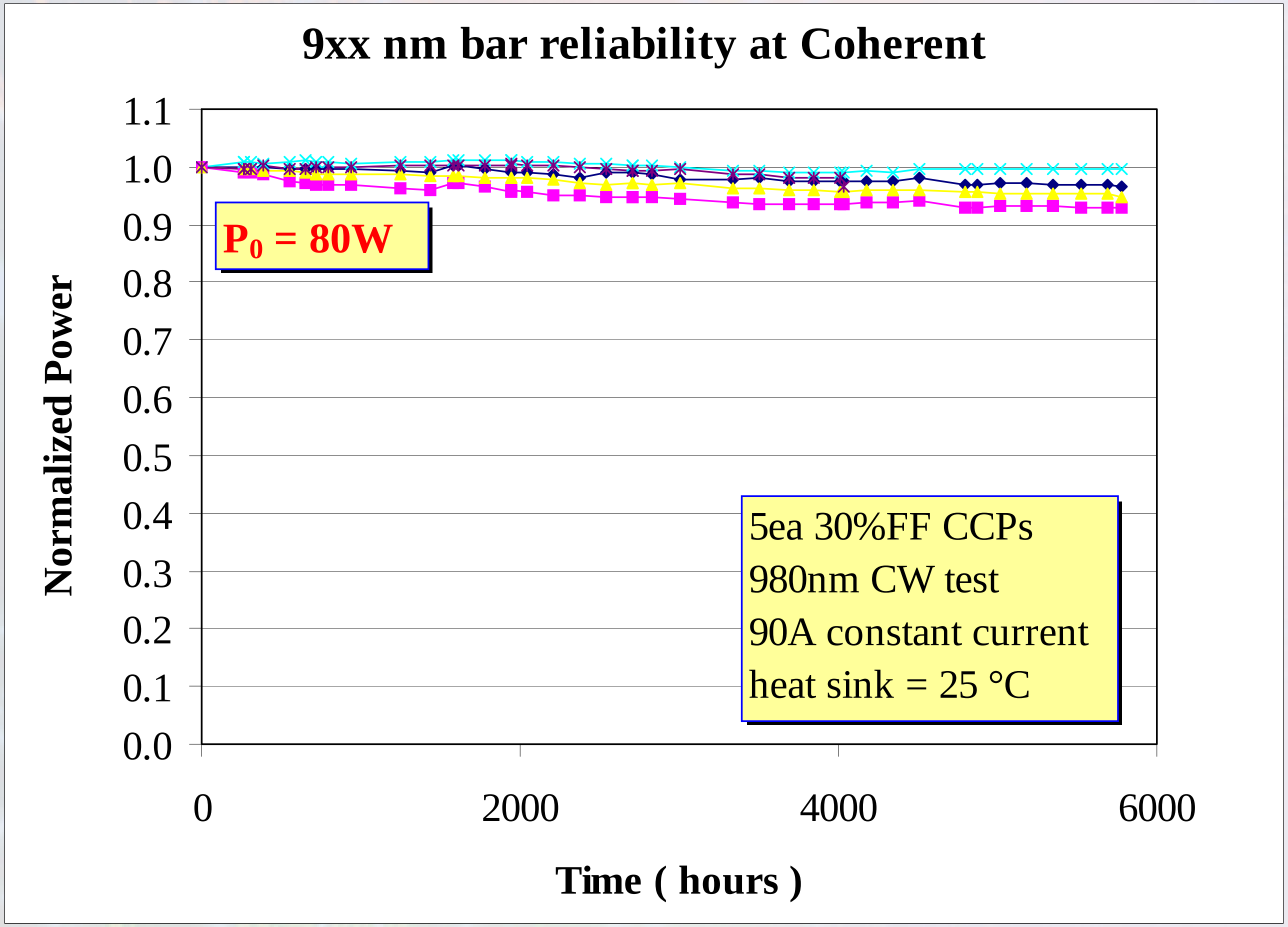


- High-temp epi-design
- 30% fill-factor bar
- PCE >60% @
  - TEC = 60°C
  - 60W CW
  - Passively cooled

Reliability of our 9xx nm bars at 50W



Reliability of our 9xx nm bars at 80W



Reliability Summary of our 9xx nm Bars

- 83 30% fill-factor CCPs have been lifetested
- power: 50-90W CW
- collected > **396,000** device hours.

- random failures:
  - calculated failure rate < 0.5% per kilo-hours
  - 90% confidence level for 30 %FF bars @ 50W

- wear-out failures:
  - Median life > 30,000 hrs (with 90% CL) at 50W CW
  - Median life > 20,000 hrs at 80W CW

Stack Technology
Conductively Cooled “G-stack” – Gen 4

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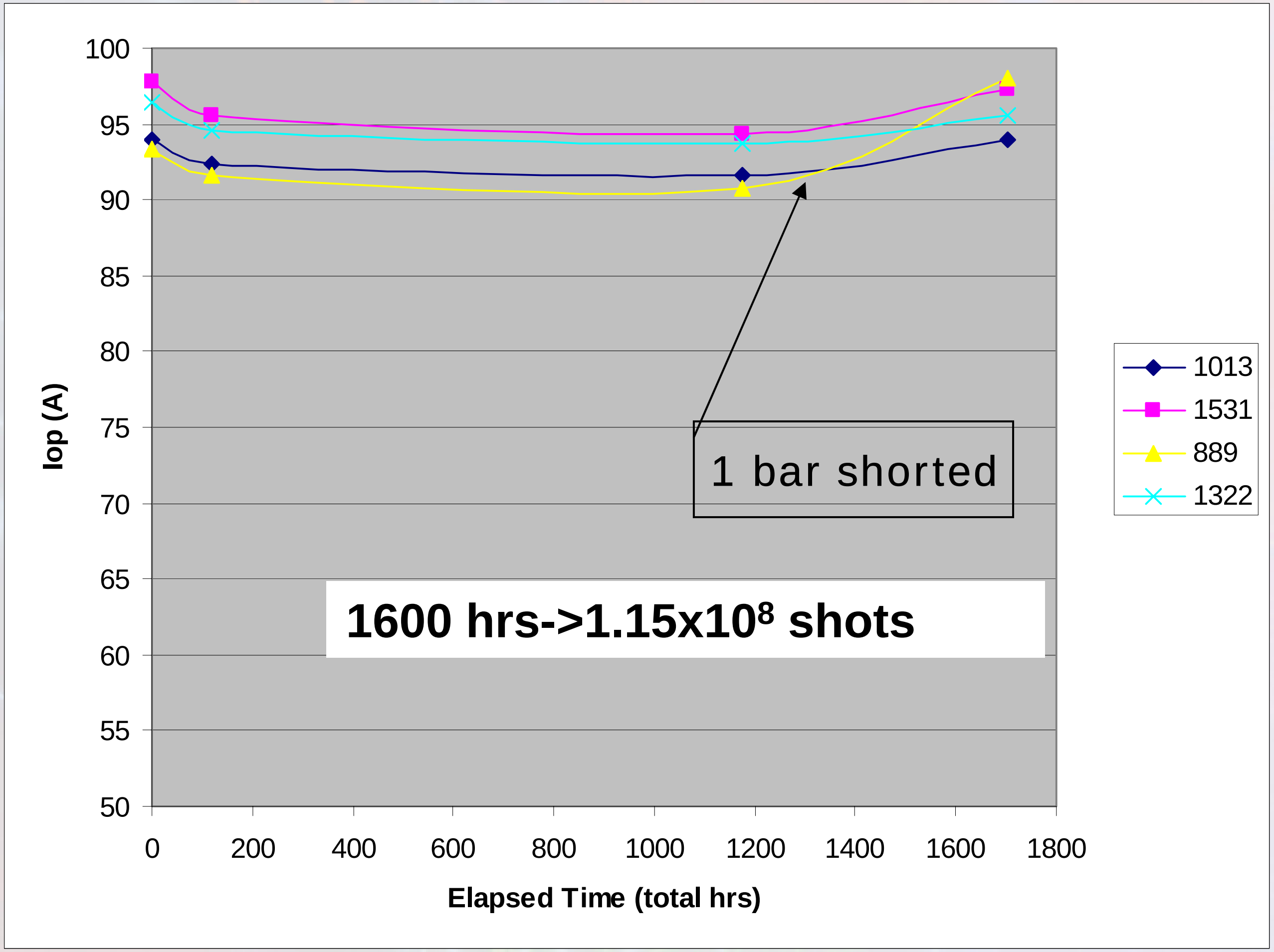
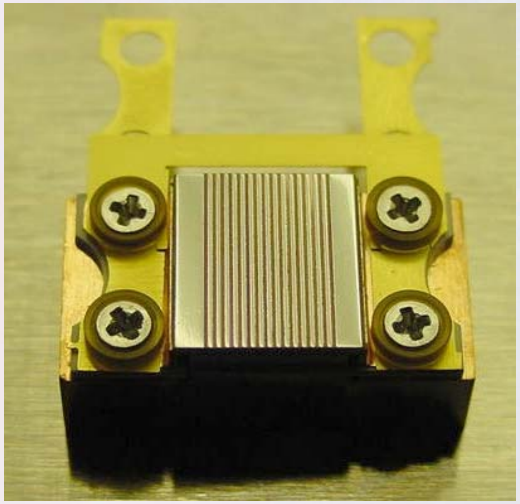
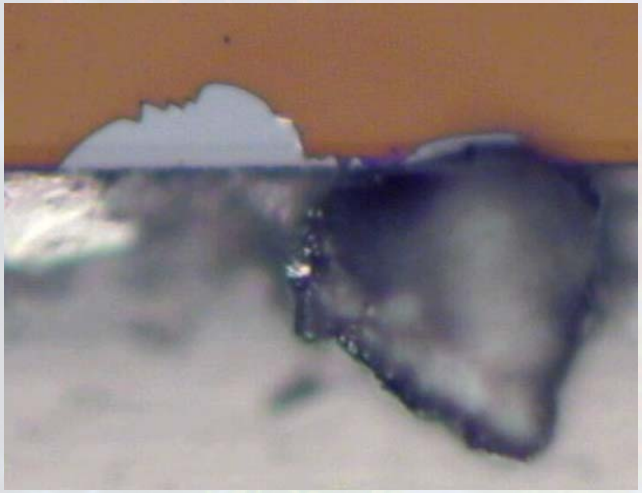
Background: Gen III G-16 Stack Lifetest at 50 °C

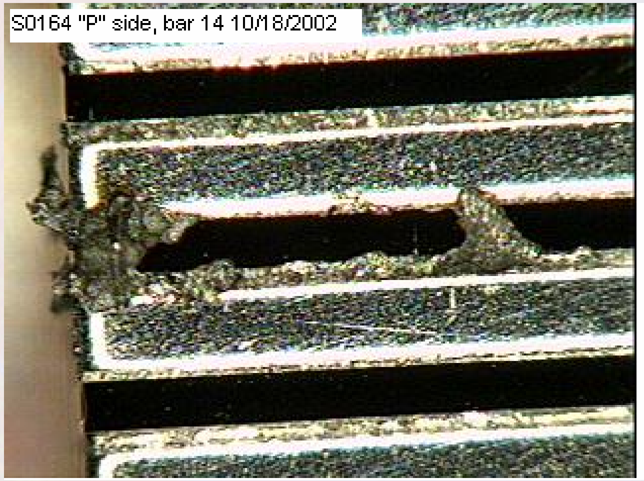




Solder Balls/Shunts

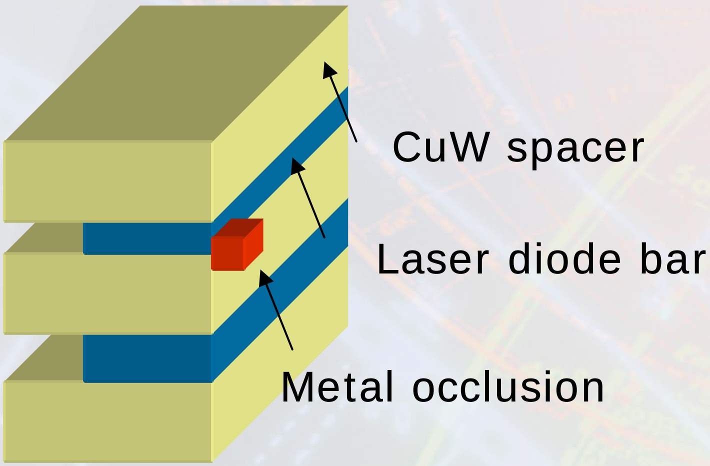


Solder ball at peel site



Solder shunts

Heating Model of a Metal Occlusion



Stack Crossection

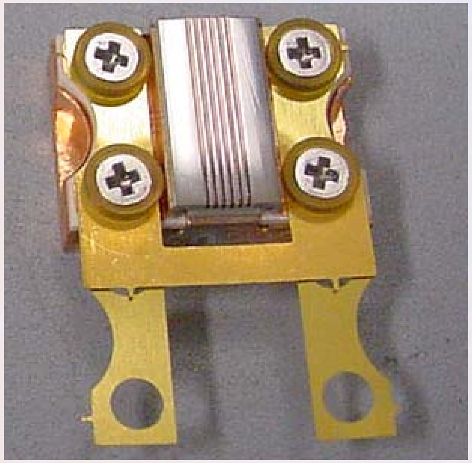
Net temperature rise

heat sink temp:	50.0°C
$\Delta t_{\text{heat sink} \rightarrow \text{sub mount}}$:	6.8°C
peak solder temp rise:	130.1°C
	186.9°C

Exceeds In-based solder reflow temperature

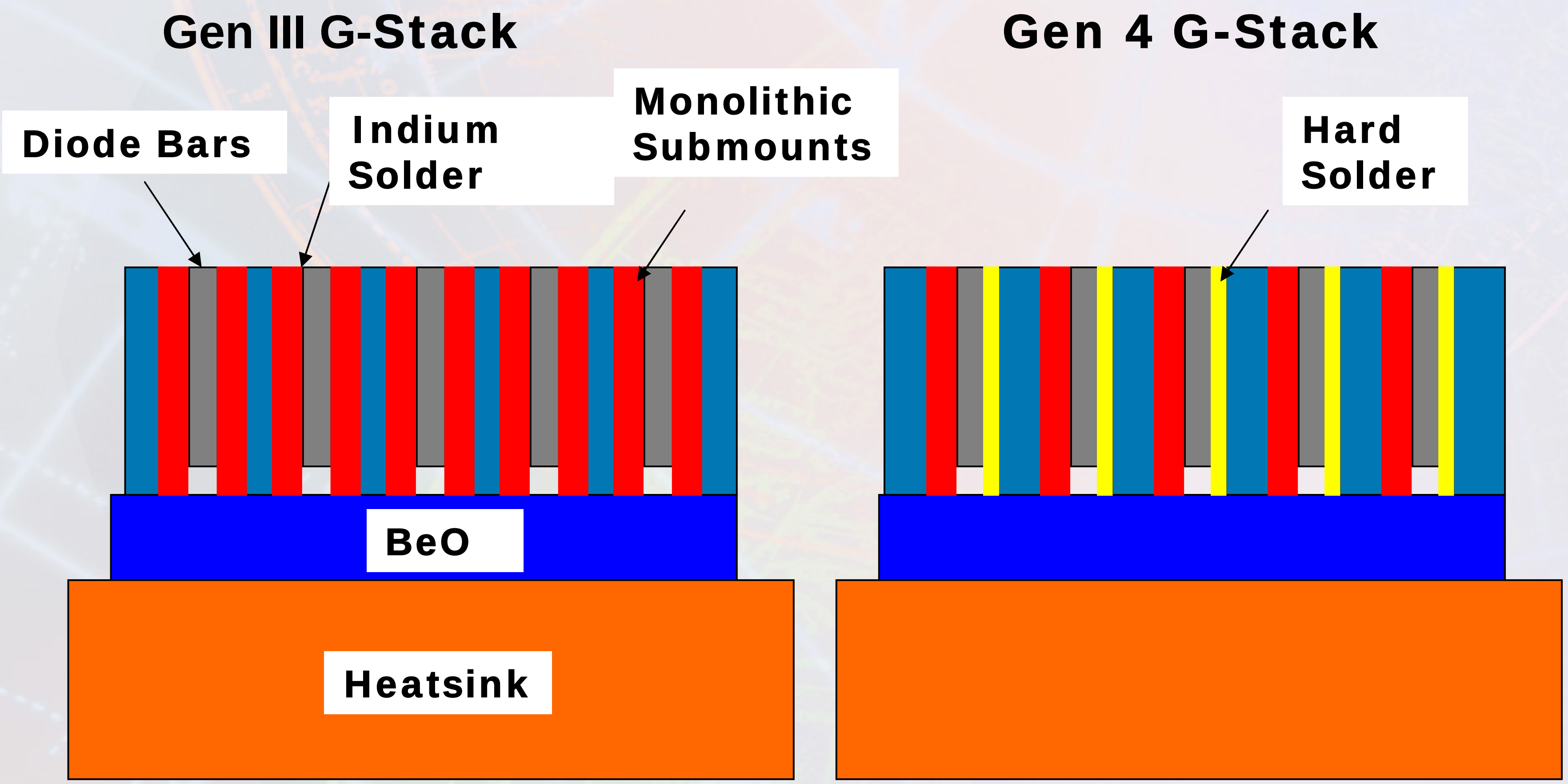
Gen 4 G-stack Development

Advantages of Hard Solder

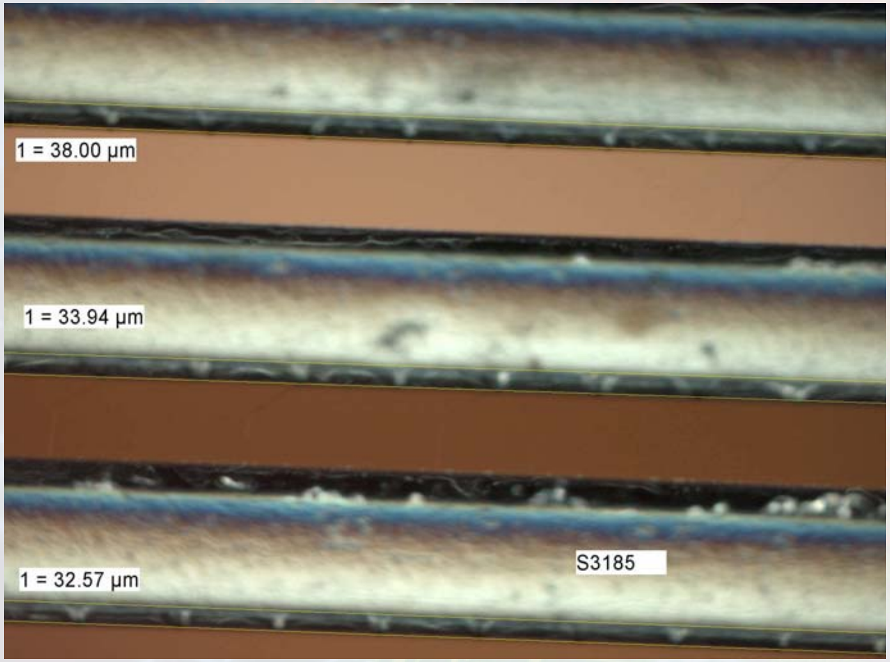


- Improves device yield
  - due to increased process window
- Improves bar to bar registration
  - consistent p-side solder volume
  - Repeatable bar preloading technique
  - Computer controlled time/temp profiles for reflow.
- Expected substantial lifetime improvement
  - substantial temperature “headroom” on p-side solder joint
  - Stable phase solder with Telecom proven reliability

Stack Assembly Methods

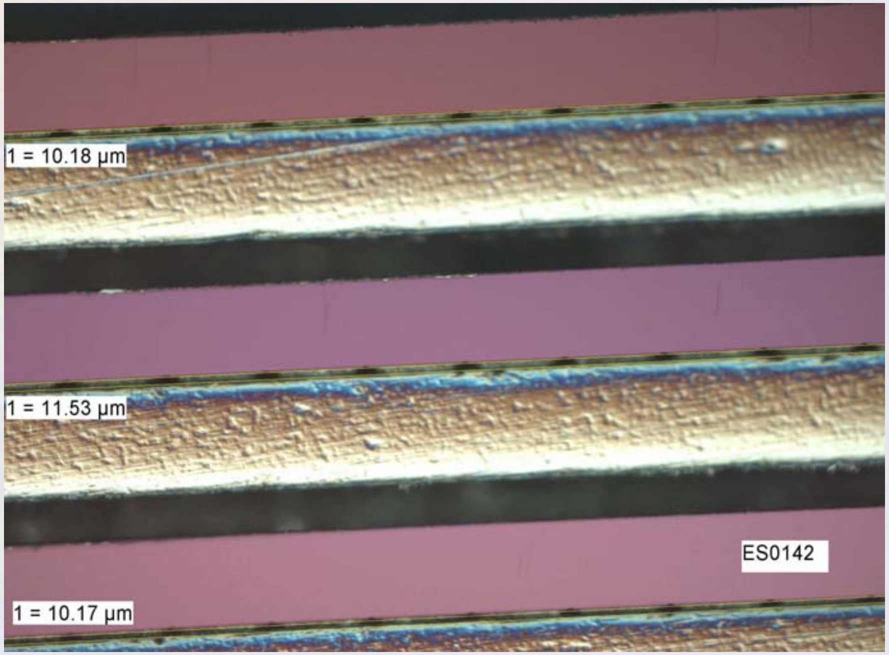


P-side solder junction thickness

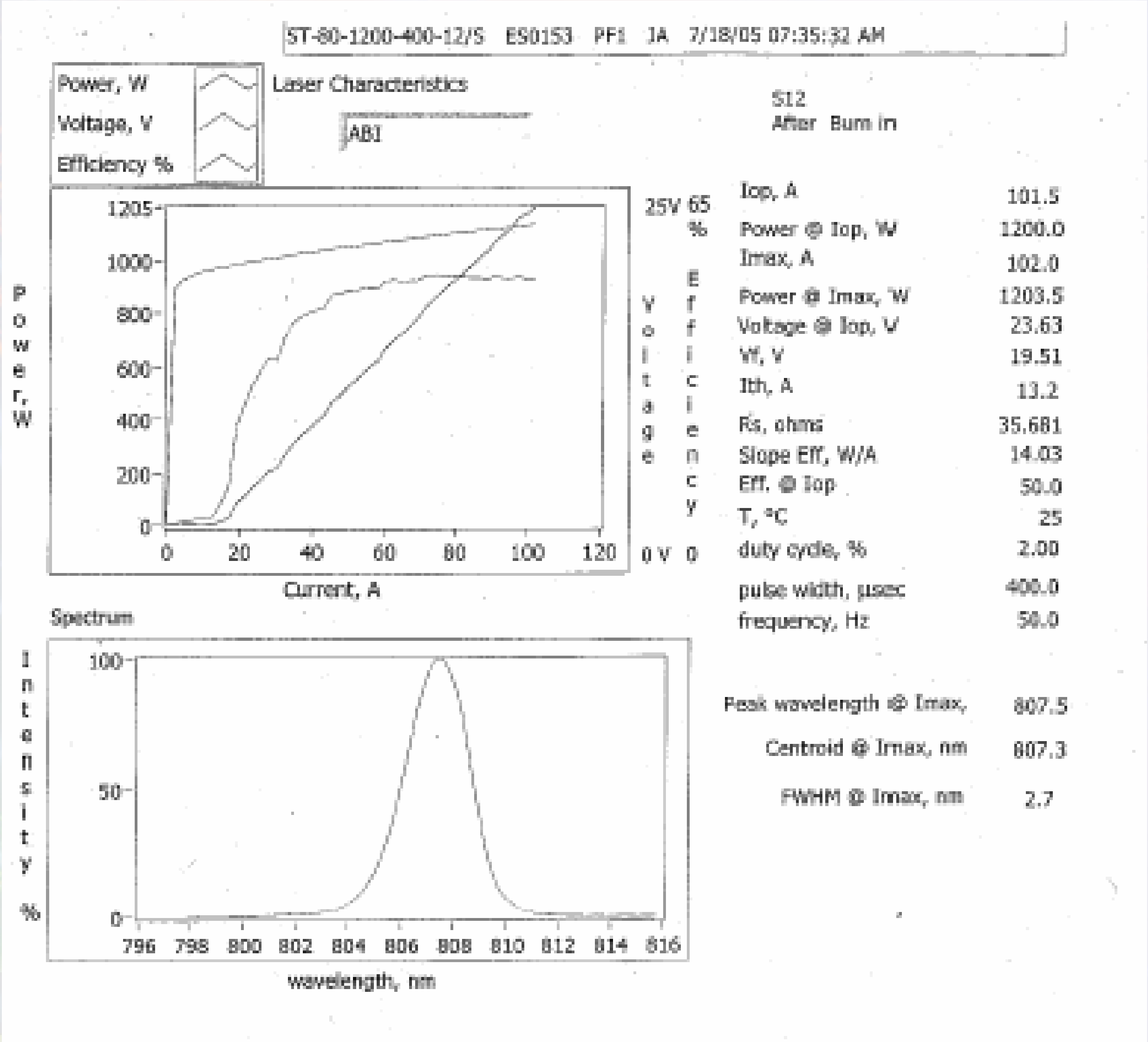


Soft Solder p-side

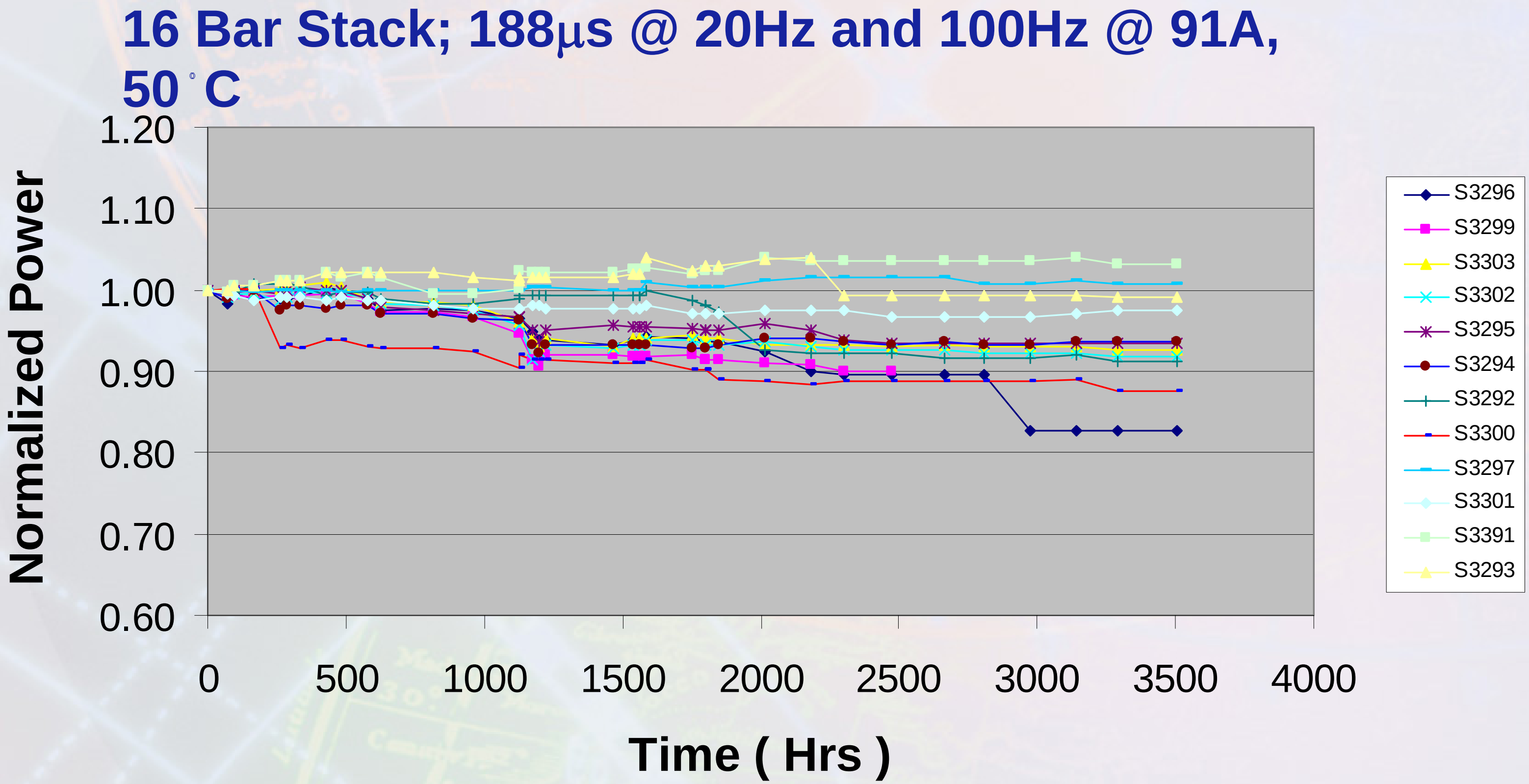
Hard solder p-side



Typical Stack PIV Spectrum



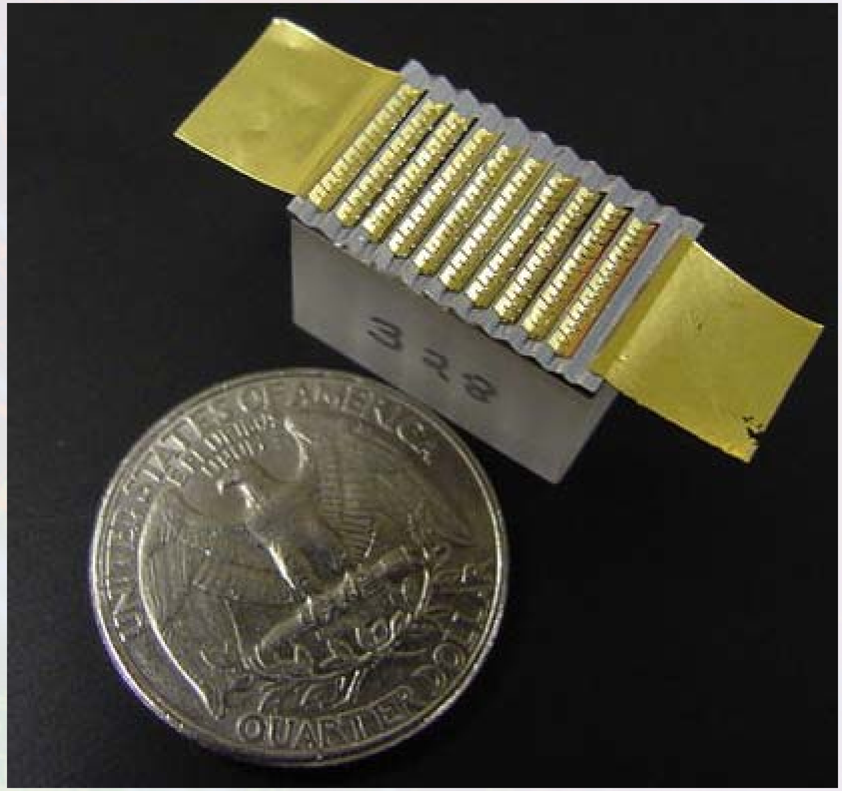
Hard Solder Stack Reliability



- **MTTF: 4.8e9 shots (90%CL)**

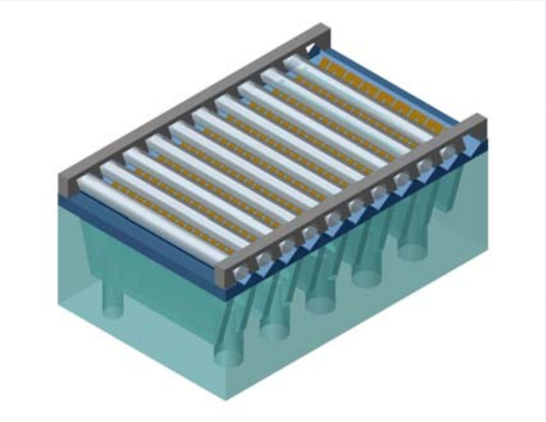
Stack Technology
Silicon Monolithic Microchannels (SiMMs)

Status of Silicon Monolithic Microchannels (SiMMs)



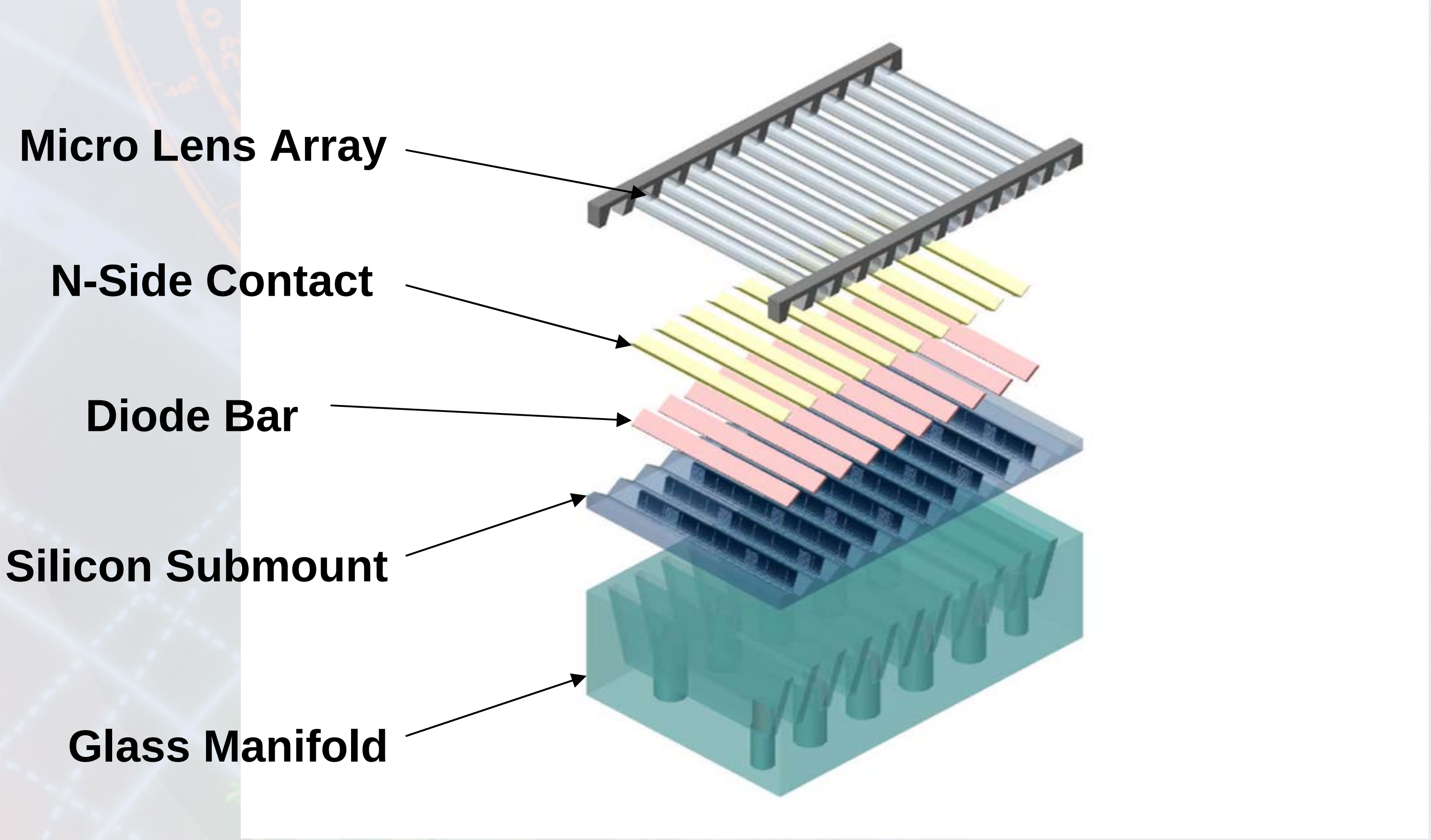
- **Technology transfer from Lawerence Livermore National Laboratories**
- **Sampling by August 2006**

What is “SiMMs”?

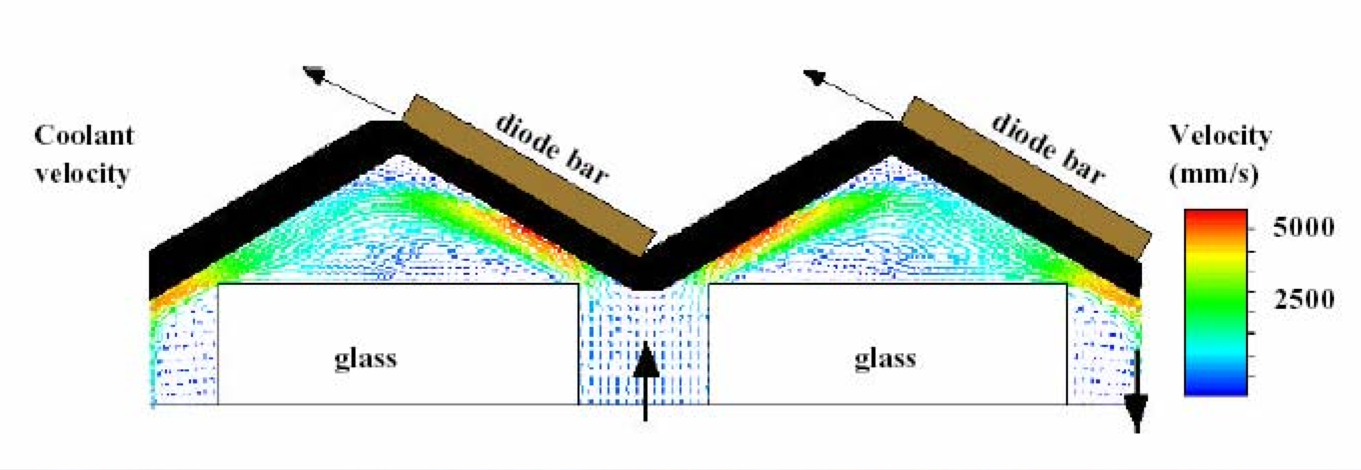


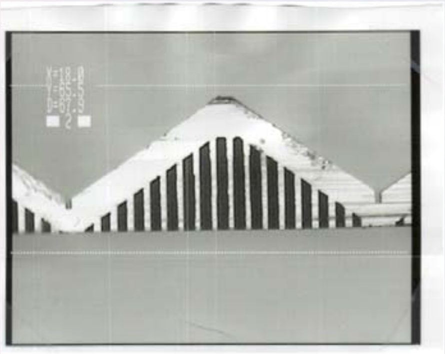
- Vertical Water Cooled Monolithic Stack
- Made from Silicon V-Groove/microchannel submount bonded Pyrex manifold (no copper)
- Optical Power-1000-1500W CW ⟶ 2000W QCW
- Lensable with Fast Axis lens array
- Low Thermal Impedance- 0.35 deg.C/W/bar

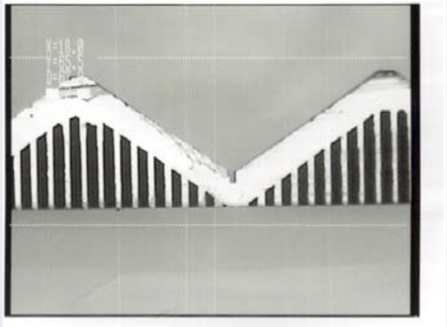
SiMMs Anatomy



SiMMs Water Flow

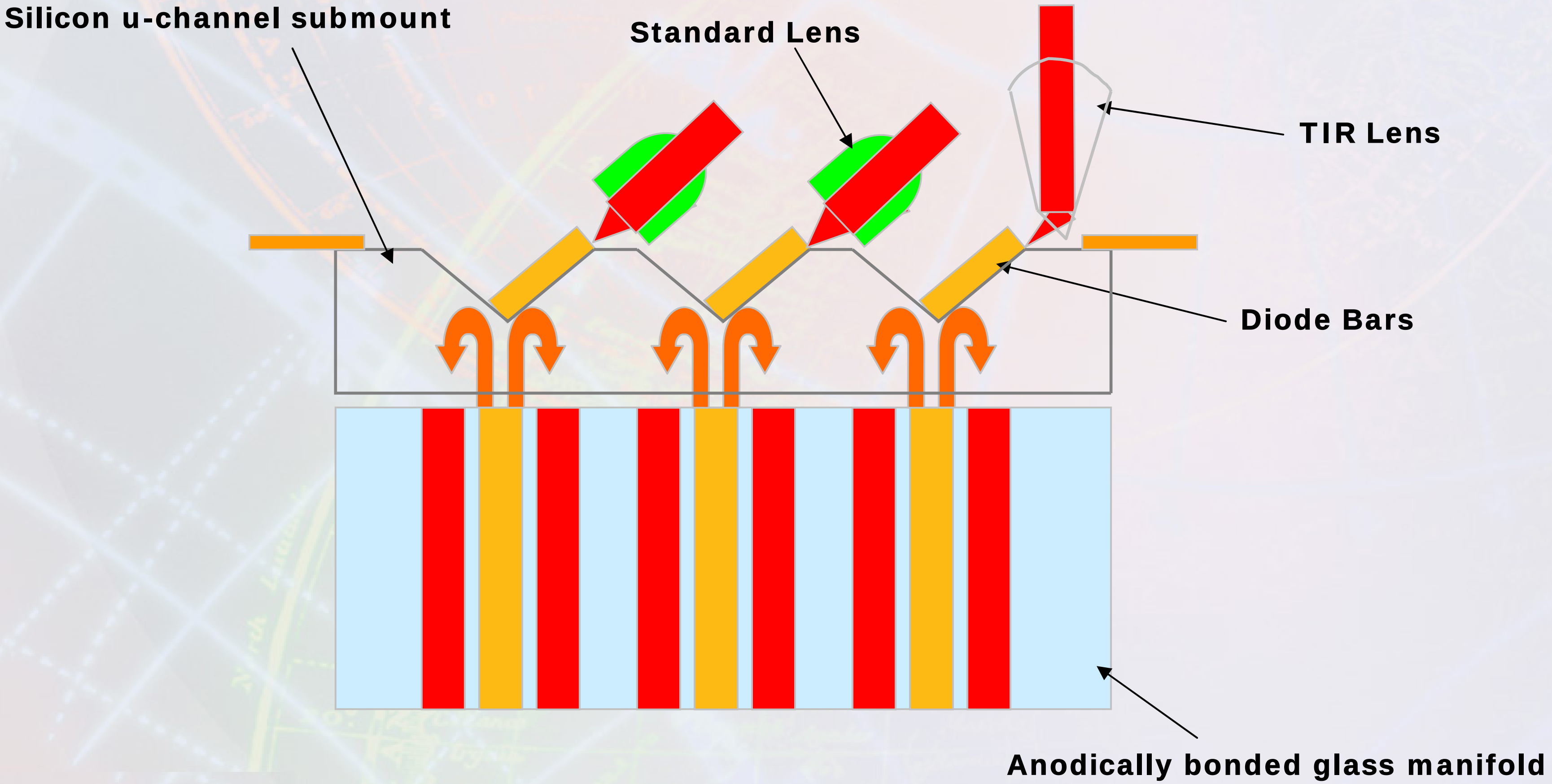






Submount Cut-Away

SiMMs Stack

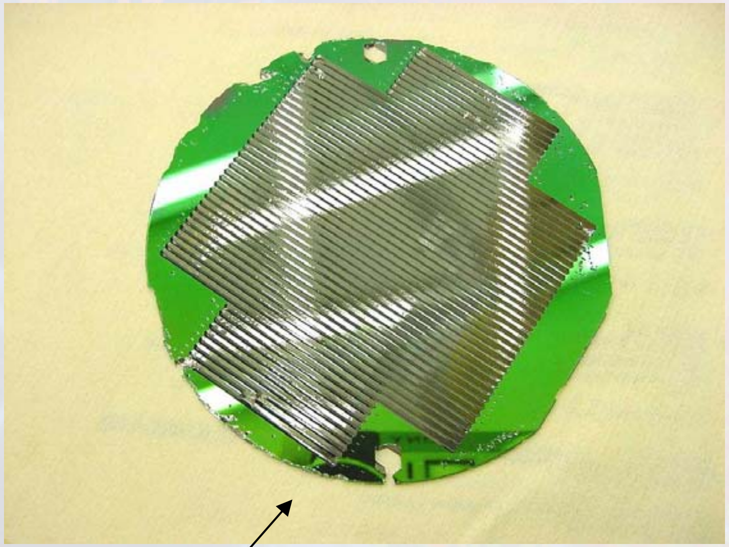


Silicon u-channel submount
Standard Lens
TIR Lens
Diode Bars
Anodically bonded glass manifold

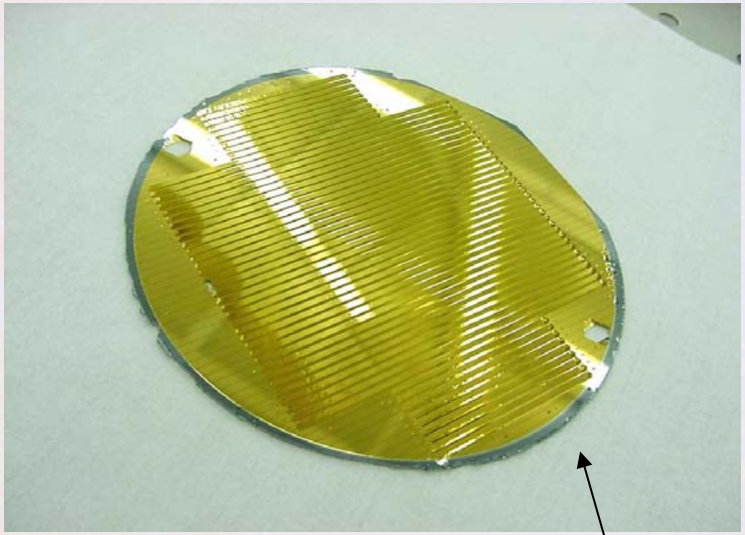
Advantages of SiMMs

- **NO COPPER**
  - Eliminates corrosion failures
  - Simple filtered water requirements for stack cooling
  - Silicon has better CTE-match for potentially improved “on-off” reliability
- **Monolithic design and low “smile” allows simplifies lensing**
  - Lens arrays using self-aligned silicon “rails”
- **Compact Footprint allows tiling of arrays**
- **Silicon-based technology should enable large scale manufacturability**
  - Lower cost

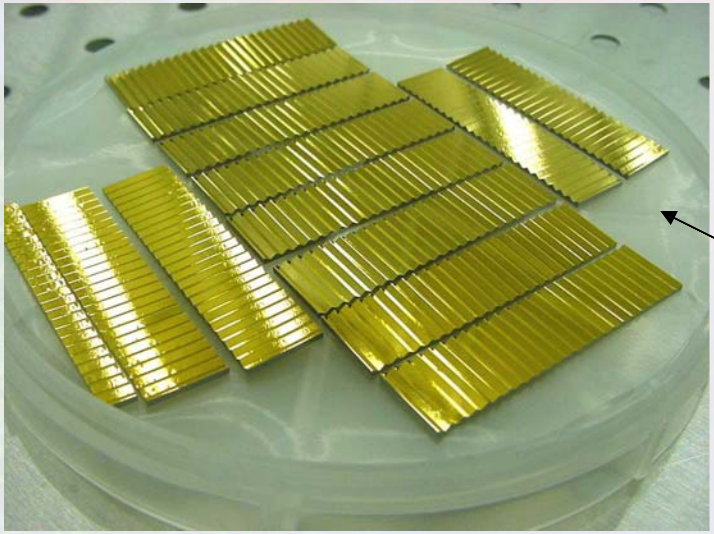
Silicon “Submount” Fabrication – Vbasis



Post KOH etching

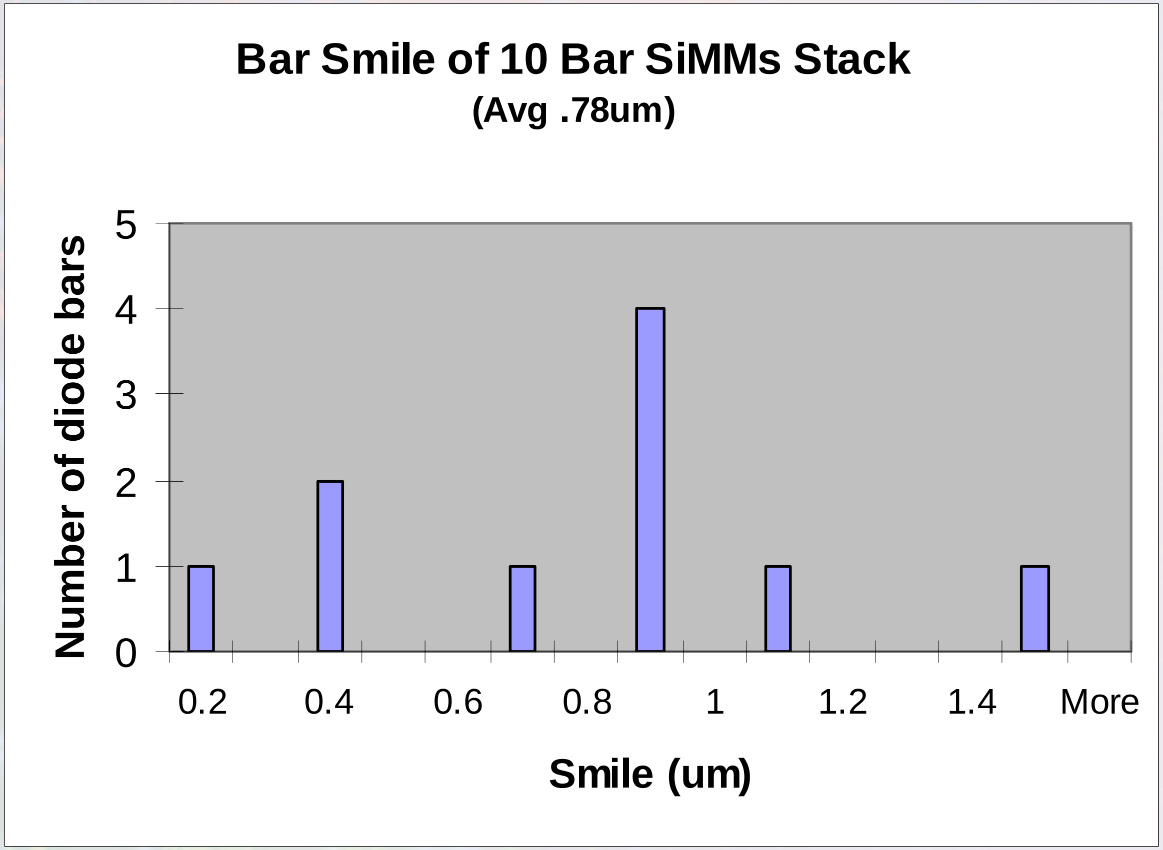


Post Metalization



Post Dicing

SiMMs Characterization - Bar Smile



- Suggests low mounting stress
- Enables easier lensing and beam shaping

808nm SiMMs Stack 15^{0}C

Pmax = 1620 Watts CW
Max Efficiency = 54%

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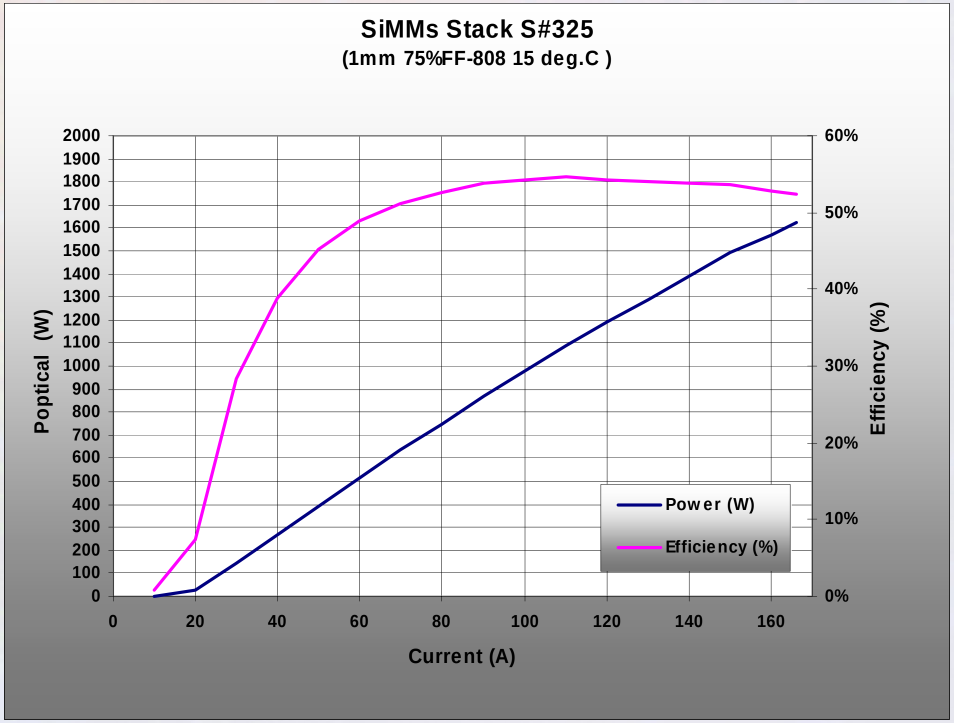
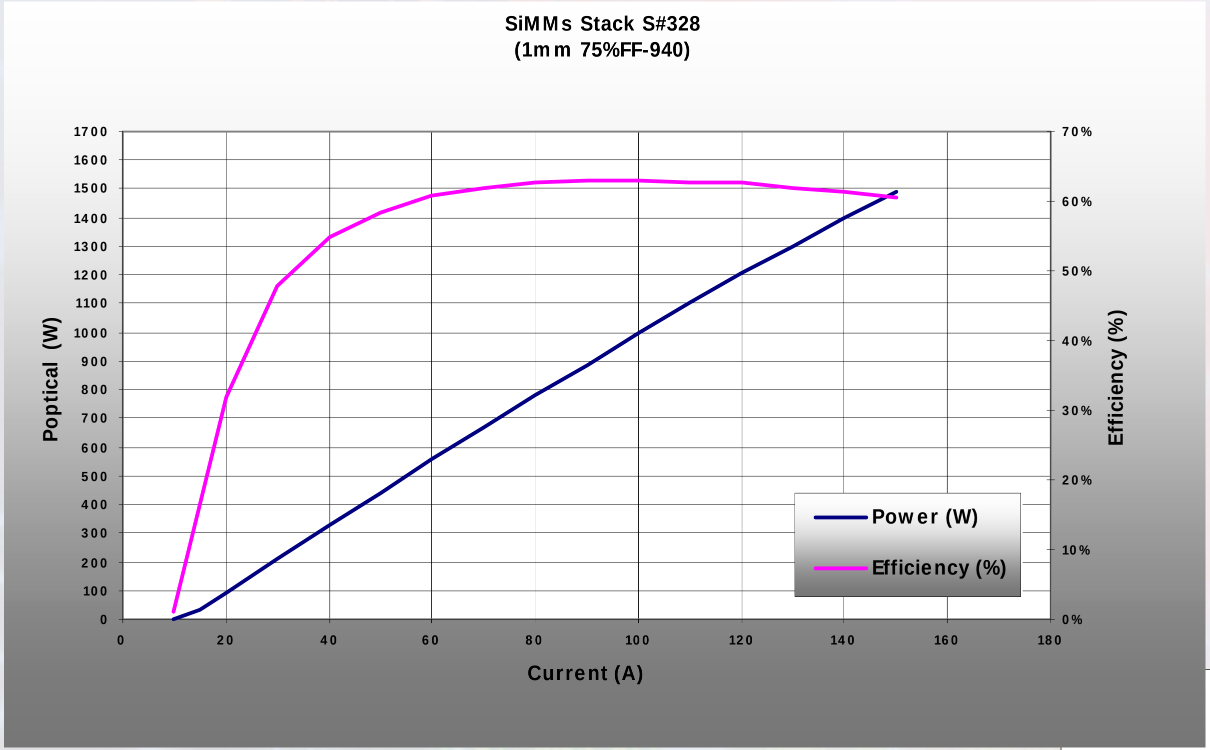
Customer	Any
SO #	
Part Number	
Serial Number	S325-10
Date	4/25/2006
P @ Imax (W)	1620
Imax	166
V @ Imax (V)	18.64
Max Efficiency (%)	55
Temperature (^{0}C)	15
Lamda @ Imax (nm)	816.64
Pressure Drop (PSI)	38
Flow Rate (LPM)	2

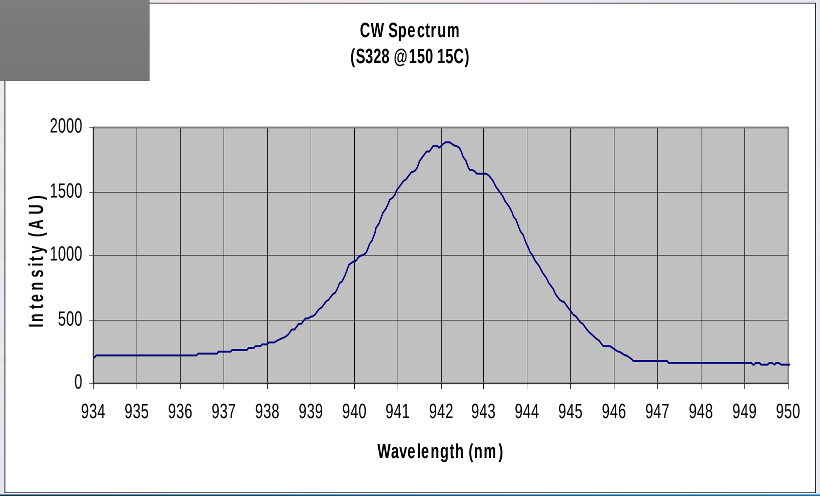
Current (A)	Voltage (V)	Power (W)	Efficiency (%)	Ctr. Wavelength (nm)	Est. Tj	Pheat
10	16.42	1.5	1%			163
20	16.75	25	7%			310
30	17.00	145	28%			365
40	17.21	268	39%			420
50	17.38	393	45%	808.24	29.9	476
60	17.54	515	49%			537
70	17.68	634	51%	809.49	34.8	604
80	17.81	750	53%			675
90	17.93	868	54%	810.66	39.3	746
100	18.04	978	54%			826
110	18.15	1090	55%	811.99	44.5	907
120	18.26	1190	54%			1001
130	18.35	1290	54%	813.49	50.4	1096
140	18.43	1390	54%			1190
150	18.53	1490	54%	815.31	57.5	1290
160	18.59	1570	53%	816.22	61.0	1404
166	18.64	1620	52%	816.64	62.6	1474



940 nm SiMMs Stack



Customer	Hailong Z.
SO #	
Part Number	
Serial Number	328-SS-10
Date	5/3/2006
P @ Imax (W)	1490
Imax (A)	150
V at Imax (V)	16.39
Max Efficiency (%)	63
Temperature (^{0}C)	15
Wavelength (nm)	942.11
FWHM (nm)	3.93
Pressure Drop (PSI)	33
Flow Rate (LPM)	2

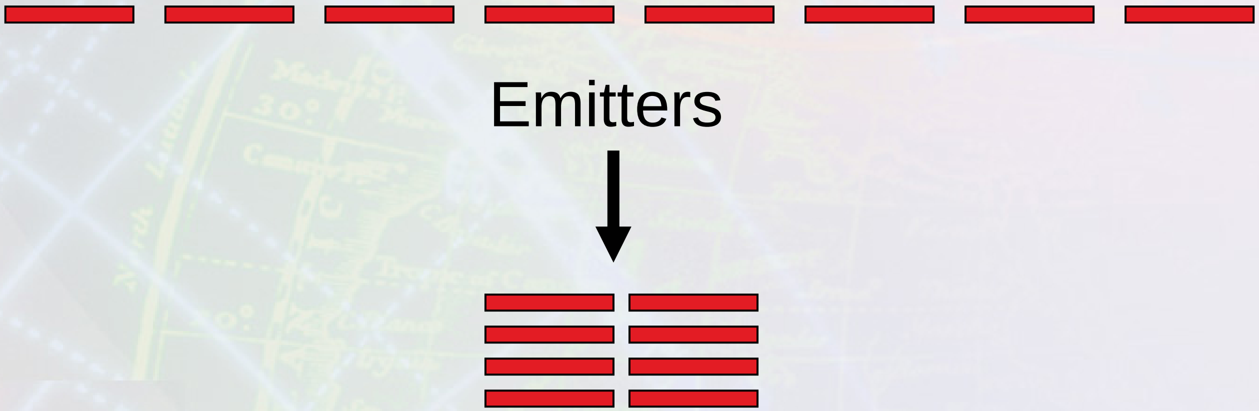


Pmax = 1500W CW
Max. Eff. = 63%

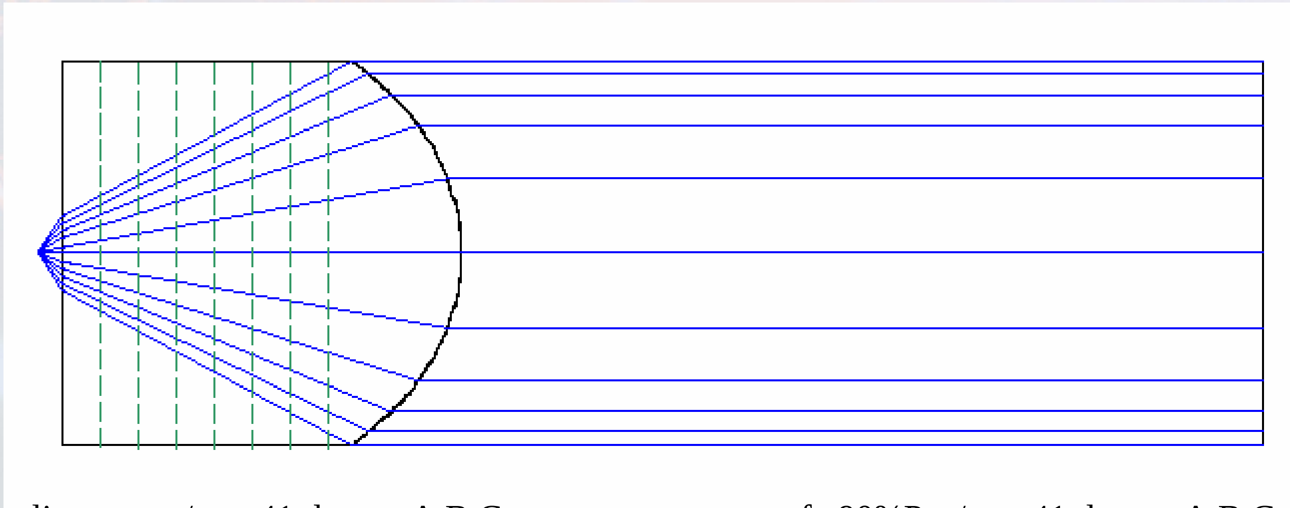
On The Horizon

On The Horizon

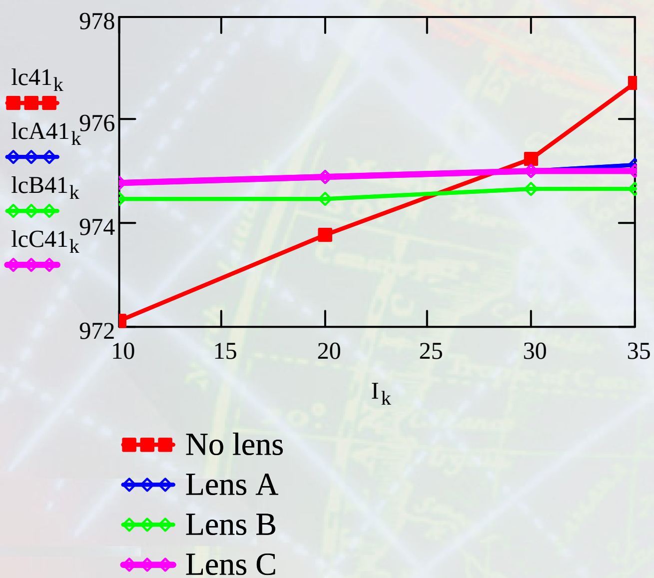
- Further Applications of “Telecom” techniques
  - “Hard Solder” SiMMs
  - No “indium” G-stacks
- Beam Combining to Increase Brightness
  - Spatial Beam Stacking (Out of a Fiber)



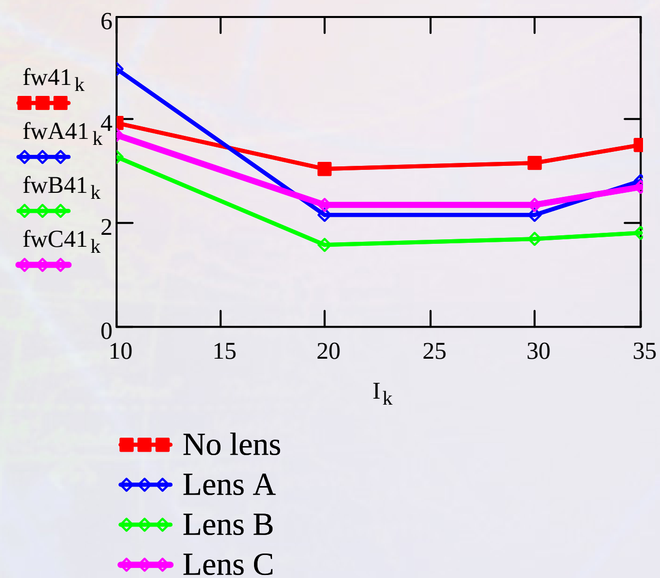
On the Horizon- Volume Bragg Grating Lens



lin centr, s/n=...41; lenses A,B,C

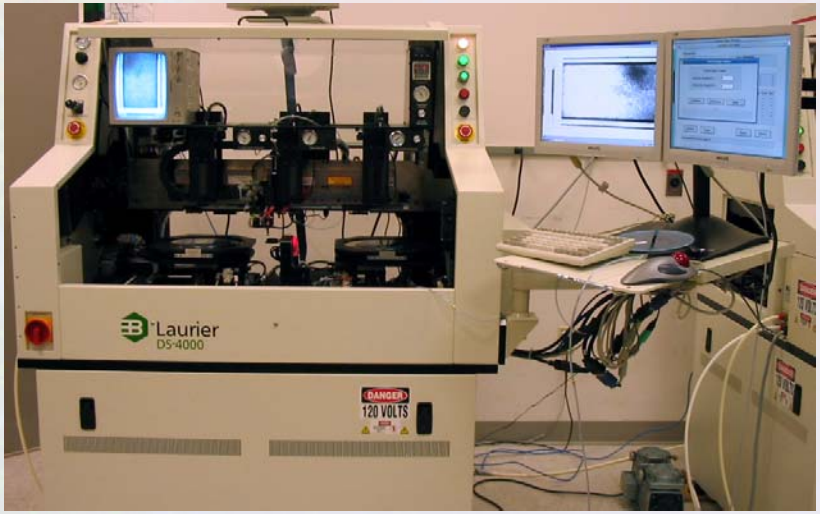


fw90%P, s/n=...41; lenses A,B,C



On The Horizon – Greater Manufacturing Efficiency

- Driven by Mantech program
- Larger wafers to reduce cost – up to 4” wafers
- Automation of bar inspection to reduce cost
- Automation of stacking/unstacking to increase yield and reduce cost



Thank You